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To cite this article: K. Kanisaukas *et al* 2017 *JINST* **12** P02010

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RECEIVED: October 21, 2016

REVISED: January 31, 2017

ACCEPTED: February 1, 2017

PUBLISHED: February 15, 2017

Radiation hardness studies of AMS HV-CMOS 350 nm prototype chip HVStripV1

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ABSTRACT: CMOS active pixel sensors are being investigated for their potential use in the ATLAS inner tracker upgrade at the HL-LHC. The new inner tracker will have to handle a significant increase in luminosity while maintaining a sufficient signal-to-noise ratio and pulse shaping times. This paper focuses on the prototype chip “HVStripV1” (manufactured in the AMS HV-CMOS 350nm process) characterization before and after irradiation up to fluence levels expected for the strip region in the HL-LHC environment. The results indicate an increase of depletion region after irradiation for the same bias voltage by a factor of ≈ 2.4 and ≈ 2.8 for two active pixels on the test chip. There was also a notable increase in noise levels from 85 e^- to 386 e^- and from 75 e^- to 277 e^- for the corresponding pixels.

KEYWORDS: Radiation-hard detectors; Solid state detectors; Si microstrip and pad detectors

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1 Introduction

Silicon tracking detectors have been central to high-energy physics experiments for the last few decades. For instance, silicon detectors were used in such experiments as NA11, DELPHI (LEP) and CDF (Tevatron) [1]. Most contemporary inner trackers use the well-known silicon hybrid detector design, where sensor and electronics are manufactured separately and then mated via bump-bonding or wire-bonding allowing both the sensor and signal processing to be optimized separately [2]. However, there has been interest for some time to integrate the signal processing circuit within the sensor substrate since it would allow the expensive hybridization process to be eliminated. Although such detectors in general produce smaller signals due to a thin depletion region, the signal-to-noise ratio is expected to be maintained due to very low input capacitances which result in low noise levels [3]. Various monolithic silicon detector concepts have been investigated since the 1980s including DEPFET, monolithic SOI, and CMOS and are starting to

find applications in high energy physics experiments [4, 5]. Monolithic CMOS prototypes which were investigated before demonstrated non-ionizing radiation tolerance to 10^{12} n_{eq}/cm^2 and had a thin (up to ≈ 15 μm) epitaxial layer that places an upper limit on the minimum ionizing particle signal (≈ 1000 e^-). The charge collection mainly relied on a slow diffusion mechanism (≈ 100 ns) [6, 7]. More recent results, however, demonstrated satisfactory radiation hardness up to 10^{13} n_{eq}/cm^2 and 1 Mrad with CMOS pixel detector prototypes developed for the ALICE experiment upgrade [8].

Recent developments in sensor technology show that commercially available High Voltage (HV) and High Resistivity (HR) CMOS manufacturing processes could potentially be utilized in producing active silicon sensors suitable for high energy physics applications [9]. A sketch of a unit cell of a HV-CMOS sensor is shown in figure 1. In this case the signal processing electronics are inside a deep n-well, whereas the depletion region forms between the deep n-well and p-substrate. The high-voltage is applied via a dedicated terminal which enables carrier drift to become a significant charge collection mechanism. The HR-CMOS process, on the other hand, utilizes a thin high resistivity epitaxial layer grown on a low resistivity substrate [10]. The ongoing developments are especially driven by the need to upgrade the inner tracker of the ATLAS experiment at the LHC. Advantages offered by detectors based on CMOS technologies include a better spatial resolution and potential reduction of the material budget and manufacturing costs.

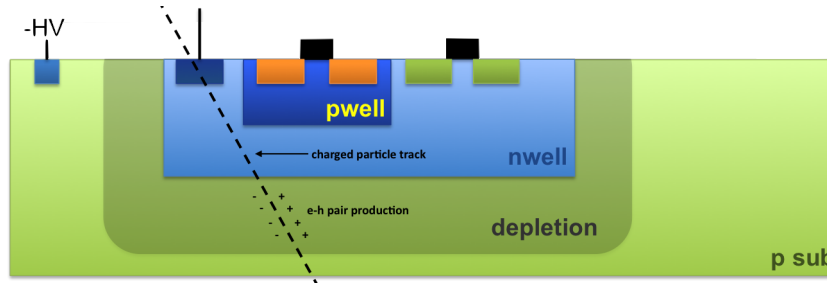


Figure 1. Unit cell of HV-CMOS monolithic active pixel sensor. The CMOS circuitry is integrated inside the n-well, while the sensitive region is formed at the interface between the n-well and a p-substrate.

The Strip CMOS collaboration was established in order to investigate the possibility to use CMOS active pixel sensors for the silicon strip tracker replacement in the ATLAS detector for the upcoming High Luminosity-LHC, which is expected to lead to a tenfold increase in integrated luminosity [11]. Radiation hardness and fast pulse shaping are two of the main requirements for new CMOS sensors to be used in the ATLAS inner tracker. The central focus of this paper is the radiation hardness of the HV-CMOS prototype chip “HVStripV1”. In addition, the response of the pixel matrix to a 15 keV microfocused monochromatic X-ray beam at the Diamond Light Source facility was evaluated before irradiation.

2 Materials and methods

2.1 AMS HV-CMOS HVStripV1

The results presented in this paper correspond to HVStripV1 test chip, which was designed at KIT [12] and manufactured in the AMS HV-CMOS 350 nm (H35) process. The p-substrate

resistivity was expected to be $\approx 20 \Omega \cdot \text{cm}$. The chip contains a matrix of 44 active strip-like pixels arranged in 2 rows and 22 columns with integrated preamplifiers. The size of each pixel is $40 \mu\text{m} \times 400 \mu\text{m}$. A diagram of the test chip is given in figure 2, where it can be seen that further signal processing components containing comparators and digital readout blocks are situated in the periphery; however, those were not used during the characterization.

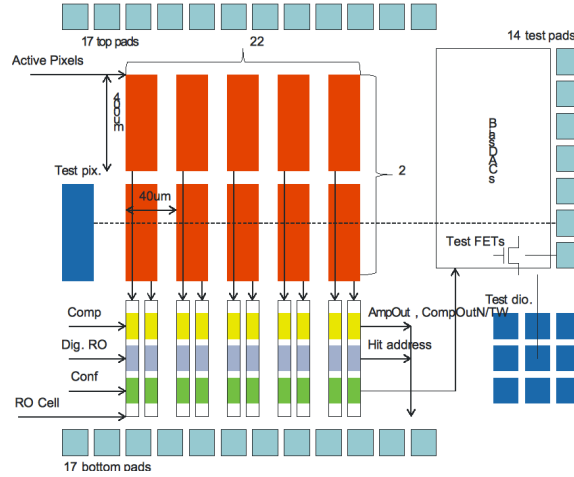


Figure 2. Diagram of AMS HV-CMOS 350 nm test chip HVStripV1. The 2 row by 22 column active pixel matrix is depicted as an array of rectangles arranged in 2 rows and 5 columns. Readout cells containing comparator, digital readout block, and configuration register are connected to individual pixels and situated below the active pixel matrix.

There are two groups of pixels within the matrix that are divided column-wise. The main difference between them is the type of transistor implemented in the preamplifier feedback circuit. One pixel group, occupying columns 0–7, has linear (regular) transistors, while another group, situated in columns 8–21, contains enclosed layout transistors [13]. The latter group was designed for enhanced radiation hardness. These different designs result in different gains being measured for the two pixel groups. The voltages and currents for the preamplifiers of the pixel matrix are set by a group of DACs. A charge injection circuit with a 0.5 fF capacitor is implemented for testing the response of the preamplifiers of the active pixels.

2.2 Data readout

The prototype chip has a single output buffer which can be connected to any given pixel in the array in order to provide an analogue output signal. This single pixel analogue output can be switched to any pixel in the array by sending the appropriate configuration sequence to the configuration register. This is achieved through a commercial Atlys FPGA board and a dedicated PCB (motherboard), to which the chip is wire-bonded. The analogue output line is connected to an oscilloscope to observe a signal. The convention used to identify a given pixel in the array is (column, row). Thus (5,0) is the sixth pixel in the top row on the left side.

2.3 Device configuration

There is a 6-bit global DAC “VNFB”, which controls the feedback resistance of the preamplifier circuit. VNFB had to be adjusted after irradiation in order to observe a signal. A higher VNFB value results in lower preamplifier gain, therefore, when comparing results before and after irradiation, this change had to be taken into account since all pre-irradiation measurements were taken using a lower VNFB value.

2.4 Laboratory measurements

2.4.1 X-ray measurements

A number of X-ray measurements were performed on HVStripV1 before and after irradiation. These measurements not only allowed the preamplifier gain of individual pixels to be extracted but also the results obtained from various X-ray sources were used to verify the linearity of response. The experimental setup was arranged as shown in figure 3. The test chip is wire-bonded on its motherboard to allow power supply and configuration of the chip. In the figure 3 it is shown that the pixel output line was connected to an oscilloscope, which itself is connected to a computer. A LabView program was written to obtain the waveforms from the oscilloscope. During data acquisition a trigger level, in the non-irradiated case, was set to $\approx 640 e^-$ and $\approx 760 e^-$ for pixels with linear and enclosed layout transistors respectively, which was ≈ 9 times above the noise level. The thresholds ensured that the vast majority of waveforms of the analogue signal correspond to X-ray induced events. 1000 waveforms were recorded at each data acquisition step.

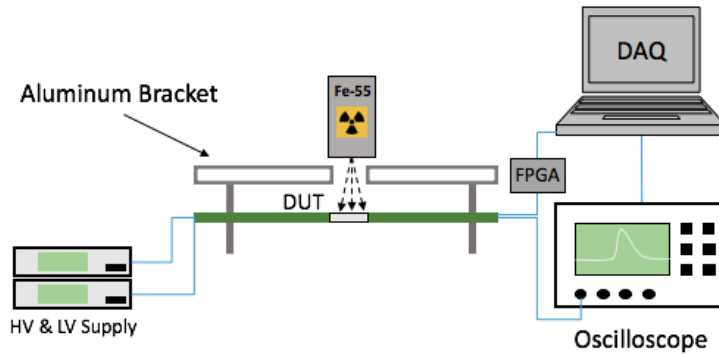


Figure 3. Illustration of the experimental setup used for X-ray measurements.

2.4.2 MIP measurements

The intended purpose of the HV-CMOS technology investigated here is for tracking detectors, therefore, minimum ionizing particle (MIP) measurements are among the most important. A Sr-90 radioisotope was used as a MIP source, since through decay chains it emits β^- particles in the MeV energy range. The average β^- energy emitted by Sr-90 is 0.196 MeV, whereas the average energy of β^- emitted by its daughter nucleus Y-90 is 0.933 MeV [14]. The experimental setup, somewhat similar to the one used for X-ray measurements, can be seen in figure 4. The main difference is a scintillator coupled to a photomultiplier tube (PMT) placed right below the test chip.

A LabView program was also written in order to record waveforms of the analogue pixel signal from the oscilloscope. In this case when triggering the data acquisition of the pixel response — the signal originating from PMT was also taken into account since the primary objective was to acquire the signal only induced by a MIP. The system was initially triggered by setting a threshold on the pixel output line as for the X-ray measurements. To select a MIP, a second trigger from the PMT was required. The secondary trigger was implemented in the LabView program, which required a PMT signal within a certain time window with respect to the pixel signal and above the background noise level.

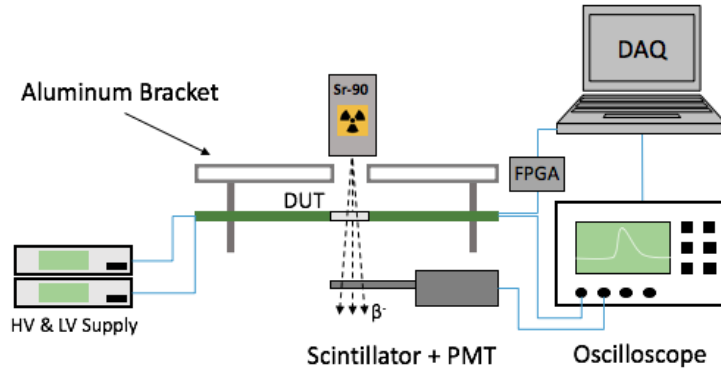


Figure 4. Illustration of the experimental setup used for MIP measurements.

The time window used was determined from prior measurements of the PMT signal versus its time of occurrence relative to the time of occurrence of the pixel signal. These measurements helped us to take into account the time walk effect because the time of occurrence ($t = 0$ s) of the pixel signal on the oscilloscope corresponds to a moment when a part of the pulse just crosses the threshold. Thus, a fraction of the pixel pulse will always stay before $t = 0$ s on the oscilloscope. How much of the pulse stays behind the time of occurrence depends on the signal height. As a consequence a coincidence PMT signal time position will shift accordingly on the oscilloscope.

The time window was set to around 200 ns depending on the pixel being tested. In majority of cases the time difference between the real occurrence of the pixel signal and the PMT signal was within tens of ns.

2.5 Diamond test beam

In addition to standard laboratory measurements, HVStripV1 was also characterized at the Diamond Light Source facility. Measurements took place at the B16 beam-line where monochromatic X-rays of 15 keV energy were available. The X-ray beam was circular with a FWHM of $2.5 \mu\text{m}$, which allowed us to perform a detailed scan of a single pixel. The test chip was mounted on translational stages positioned in the path of the beam. The signal was acquired using an oscilloscope as was done for the other measurements. A reverse bias of 60 V was applied at all times. Depending on the type of measurement, either the number of hits over threshold within a fixed time-frame or a preamplifier signal peak value was recorded.

2.6 Irradiation at Birmingham

Radiation hardness is one of the most important characteristics of HV-CMOS technology investigated in this paper. Two HVStripV1 samples were irradiated at the MC40 cyclotron facility at the University of Birmingham. A proton beam of 27 MeV energy was used for irradiation. The device arrangement can be seen in figure 5, where part of the setup was placed inside the “cold box”. The purpose of the cold box was to provide a cold and dry environment for the test devices in order to control annealing. Low temperature in the cold box was maintained by a constant supply of liquid nitrogen. An aluminum bracket was designed to accommodate two test chips so that both could be irradiated in a single campaign. In the diagram it can be seen that there is vertical offset between two chips; however, since the cold box itself was placed on translation stages the chip position was alternated during the irradiation. The irradiation procedure consisted of five 1000 s proton beam periods allocated for each test device to achieve target fluence of $1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. The motherboards were shielded with a layer of aluminum, thus only the test chips were exposed to the beam. In addition, PT100 sensors were attached as close as possible to the chips in order to monitor temperature during irradiation.

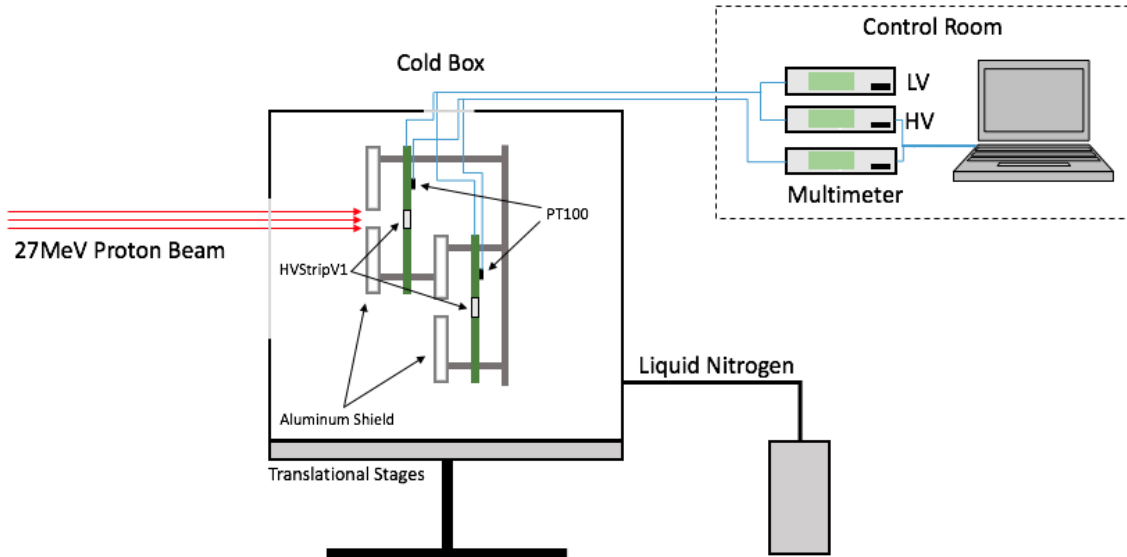


Figure 5. Experimental setup during HVStripV1 irradiation at MC40 cyclotron facility. The translational stage moves vertically allowing exposure to each device in turn.

The chips were powered and two different reverse bias voltages of 40 V and 20 V were supplied to the different chips at all times. Power and high voltage supply units, together with multimeters for temperature measurements, were placed in the control room. A LabView program was written to log temperatures and leakage currents of both devices. The communication between PC and corresponding units was established via a GPIB interface. The temperature on the PT100s remained stable at $-52 \pm 1.6^\circ\text{C}$ during irradiation. The final fluences achieved corresponded to $1.0 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ and $1.2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$.

3 Results and discussion

3.1 Before irradiation

3.1.1 Diamond test beam results

A number of measurements were performed at the Diamond Light Source (DLS) facility before irradiating test devices. The same set of measurements was not repeated after irradiation. In addition, the test chip characterised at the DLS facility does not correspond to the same device for which the results are presented below. The results presented demonstrate charge collection across a single pixel and the response of the entire pixel matrix to a 15 keV X-ray beam.

Pixel X-Y scan. The first set of results include a detailed scan along two dimensions of a single pixel. The scan was done after identifying beam position and focusing it to $2.5\text{ }\mu\text{m}$ of width. A pixel with a linear transistor was selected for the measurements. The reverse bias was set to 60 V. While the scan was performed on one coordinate the other was kept constant at the central position of the pixel. In order to optimize the data acquisition different step sizes were chosen along width and length of the pixel i.e. $2\text{ }\mu\text{m}$ and $10\text{ }\mu\text{m}$ steps were chosen along $40 \times 400\text{ }\mu\text{m}^2$ pixel dimensions respectively. During the measurements a number of hits over 2450 e^- threshold in 1 ms time-frame was recorded at each step. A charge deposited by 15 keV photons in the sensor corresponds to $\approx 4170\text{ e}^-$. The results are shown in figure 6, where the pixel response pattern matches well with the pixel dimensions. The estimated FWHM along X-coordinate corresponds to $36\text{ }\mu\text{m}$, whereas along Y-coordinate - $395\text{ }\mu\text{m}$. The values correspond to 90% and 99% of the specified pixel dimensions accordingly.

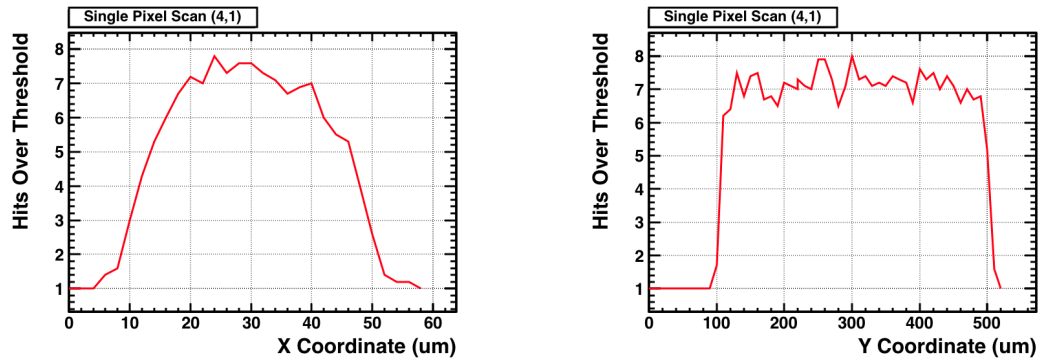


Figure 6. X-ray scan results of a pixel with a linear transistor in both dimensions. It can be seen that the response pattern is close to expected $40 \times 400\text{ }\mu\text{m}^2$ pixel dimensions.

Response map. The next step was to acquire the response for the whole active pixel matrix of the test chip. For this measurement the X-ray beam was positioned at the central position of each pixel. The reverse bias was kept at 60 V. Peak values of the preamplifier signal were recorded for every pixel in the matrix. The results for all pixels are shown in figure 7. In the response map two pixel regions can be clearly distinguished since pixels from column 0 to 7 have higher gain than the rest of the matrix. The results were later used to determine the gain of individual pixels. For pixels with linear transistors in the preamplifier feedback circuit the average gain was found to be

237.5 ± 12.7 mV/fC, whereas the average gain of the pixels with enclosed layout transistors was 176.1 ± 15.8 mV/fC. The average gain values, although somewhat similar, are not the same as the ones presented in the linearity of response before irradiation section below since in this case the measurements were performed for a different device. The larger spread in gain values among the pixels of the same group could potentially be attributed to the X-ray beam position not being in exactly the same position for every pixel since the beam position had to be adjusted manually.

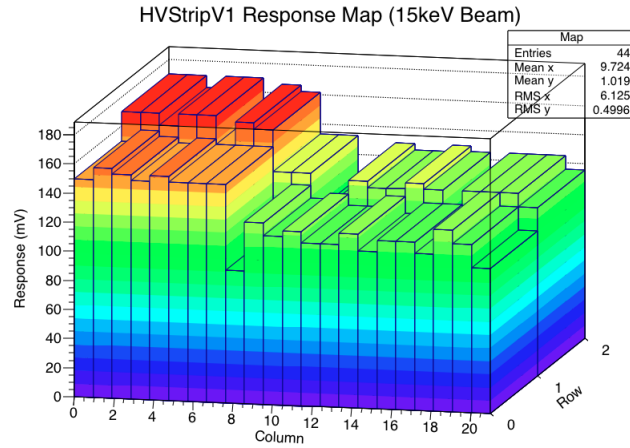


Figure 7. Response map of HVStripV1 active pixel matrix to 15 keV photons. Two different pixel groups can be clearly distinguished. Pixels situated from column 0 to 7 correspond to pixels with linear transistors, while the ones situated from column 8 to 21 correspond to pixels with enclosed layout transistors.

3.1.2 Linearity of response

An important characteristic of any detector designed for particle physics applications is its linearity of response. In order to evaluate this for preamplifiers of the active pixel matrix, two methods were employed — charge injection and variable X-ray source measurements. For the first method a pulse generator was connected to the charge injection circuit and the pixel outputs were recorded for an input pulse height range of 0.5–2.5 V. Although the specified capacitance in the injection circuit is 0.5 fF, using X-ray data the measured capacitance was found to be 0.62 ± 0.03 fF. Therefore, the equivalent injected charge corresponds to $1900\text{--}9400 e^-$. The measurement of the injection capacitance relied on the assumption of full charge collection from X-rays. The same bias voltage was applied to the test device for the X-ray measurements (used to extract the injection capacitance value) and the charge injection measurements presented below.

A reverse bias of 60 V was applied to the test device. The measurements were performed for all the pixels and results of one row are given in figure 8. It can be seen that the preamplifier response is linear for pixels with linear and enclosed layout transistors. By fitting a first order polynomial to the data, gain values were obtained for all the pixels. The average gain value of the pixel group with linear transistors was found to be 247.2 ± 11.4 mV/fC, whereas average gain of the pixel group with enclosed layout transistors was 198.2 ± 8.6 mV/fC. The errors on the gain values indicate uniformity of response of each pixel group.

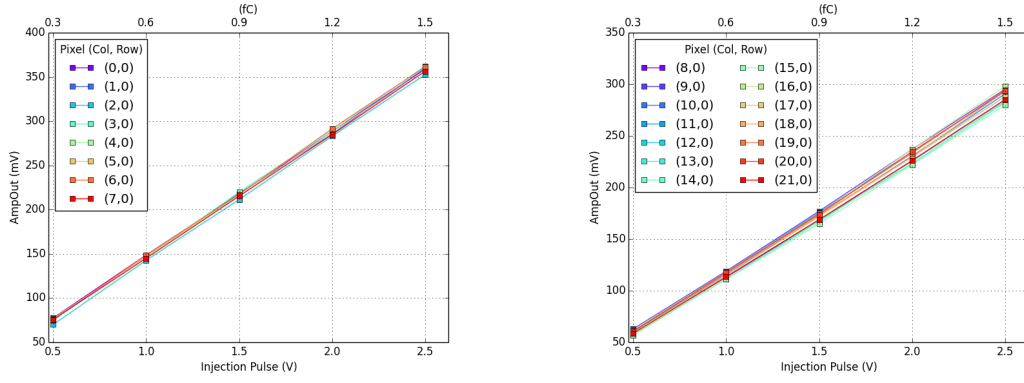


Figure 8. Measurements of preamplifier response to charge injection. Y-axis indicates peak values of the pixel output pulse. Figure on the left represents pixel group with linear transistor, and the right figure shows the results of the enclosed layout transistor pixel group.

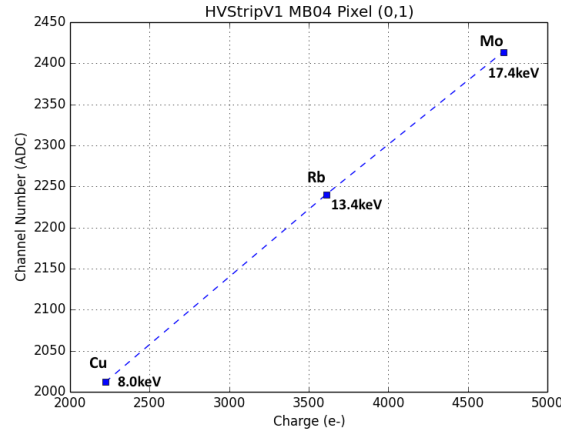


Figure 9. Linearity of pixel response to X-ray sources of various K_{α} peak energies. X-axis was converted to equivalent deposited charge by photons using a conversion factor of 3.6 eV/e-h [15].

A variable X-ray source, which had several target metals, was used to confirm linearity of response for one of the active pixels. Measurements were performed only for a single pixel due to time limitations as the source activity was relatively low which resulted in an event rate of ≈ 0.05 Hz in the pixel. The experimental setup was identical to the one given in figure 3, with the exception that instead of an oscilloscope a multi-channel-analyser (MCA) was used to acquire data. Similarly to the previous set of measurements a reverse bias of 60 V was applied. The characteristic K_{α} lines of Cu (8.0 keV), Rb (13.4 keV) and Mo (17.4 keV) were observed for a pixel with a linear transistor and the results are presented in figure 9.

3.1.3 Response to Fe-55 source

Another set of measurements were performed using an Fe-55 radioactive source, which emits X-rays with a characteristic peak of 5.9 keV energy, corresponding to $\approx 1640 e^{-}$ of deposited

charge in the detector. The deposited charge is close to the induced charge expected by minimum ionizing particles (MIPs) assuming a depletion region of $\approx 20\text{ }\mu\text{m}$. Thus, several characteristics of active pixels, including gain and signal-to-noise ratio (SNR), can be extracted using a single set of measurements. Fe-55 spectra were obtained for two pixels of different types. The variation of the peak position as a function of bias voltage was also investigated. The experimental setup used for characterization is depicted in figure 3. The values of pixel gains were extracted by fitting a

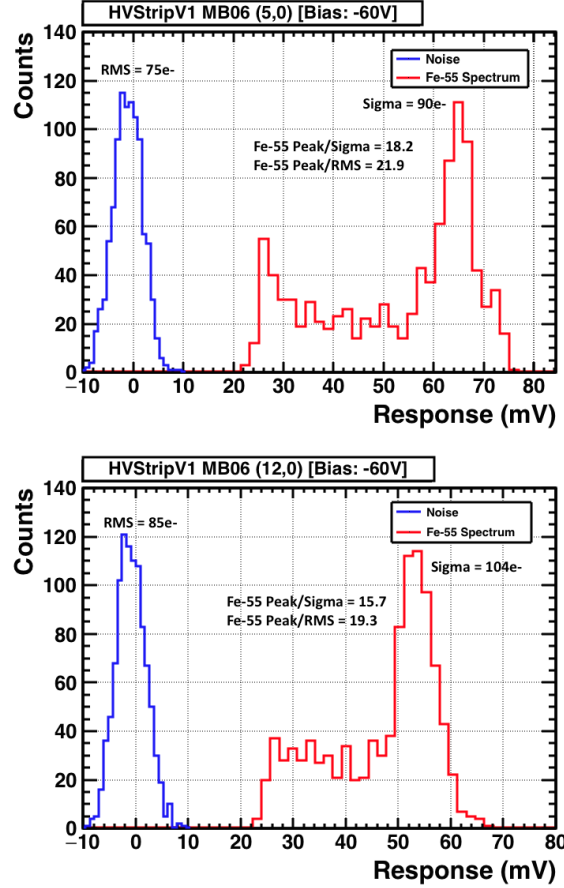


Figure 10. Fe-55 and noise spectra obtained for two types of pixels. The upper plot is from a pixel with a linear transistor, while the lower is from a pixel with an enclosed layout transistor. The Fe-55 characteristic peak is prominent for both pixels. The origin of the rest of F-55 spectrum could possibly be attributed to charge diffusion.

Gaussian to the characteristic peak of the X-ray source spectra. The results for both pixels at 60 V reverse bias are given in figure 10. The histograms also contain spectra of noise that were extracted from the same dataset. The noise was sampled at a fixed position (before the rise of pulse due to X-rays) in each waveform. The noise values were found to be 75 e^- and 85 e^- for a pixel with a linear transistor and for a pixel with an enclosed layout transistor respectively. The SNR estimate was calculated by taking ratio of peak position to the measured value of the noise. The value found for a pixel with a linear transistor corresponds to 21.9, whereas for a pixel with an enclosed layout transistor the SNR was found to be 19.3. The widths of the Fe-55 peaks are slightly bigger than

the noise values as one would expect since there is an additional statistical fluctuation in the charge deposition in the sensor.

For the same pixels gain values were obtained using the data taken and correspond to 245 mV/fC and 205 mV/fC. The peak position was found to shift to higher values with increasing bias voltage. Over 10 V to 70 V reverse bias range, the peak position increased by 13.5% for a pixel with a linear transistor and by 14.5% for for a pixel with an enclosed layout transistor. Although not presented in this paper, the same effect was observed during studies of charge injection (using the charge injection circuit) as a function of bias voltage. This is not expected for an X-ray peak and for any other means of introducing a fixed amount of charge in the sensor but was believed to be due to the effect of the change of capacitance on the gain of the preamplifier. In order to confirm the previous further studies are needed.

3.1.4 MIPs

MIP spectra were acquired for the two types of pixels within 10 V–70 V reverse bias range at room temperature. The experimental setup described earlier is illustrated in figure 4. In order to extract MIP peak position, the spectrum of each pixel was fitted with a convolution of a Landau and Gaussian distributions. The parameter extracted from the fit, which determines the peak position, is referred to as most probable value (MPV). The MPV gives an indication of the collected charge and the thickness of the sensitive region of the detector [16]. The calibration based on X-ray measurements was used to convert the pixel output peak value to deposited charge in e^- .

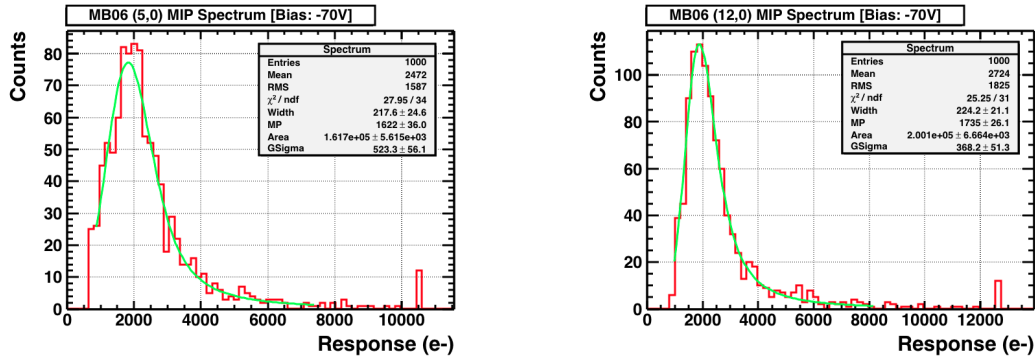


Figure 11. MIP spectra acquired at 70 V reverse bias for a pixel with a linear transistor (left) and for a pixel with an enclosed layout (right) transistor. The MPVs are close to the ones expected from a sensor with $\approx 20 \mu\text{m}$ depletion depth assuming 76 $e^-/\mu\text{m}$ [17] charge induction by a MIP.

Spectra for a pixel with a linear transistor and for a pixel with an enclosed layout transistor are shown in figure 11. The MPV at 70 V bias for these pixels corresponds to 1622 e^- and 1735 e^- respectively. In addition, a dependence of MIP peak position as a function of bias voltage was observed for a pixel with a linear transistor. It was determined that over 10 V–70 V the MPV increased by 24% for the latter pixel. In this case the calibration obtained from X-ray data was used for each bias voltage. Thus, the earlier observed effect of gain change with bias voltage was subtracted. A variation of depletion region with bias voltage is expected for a p-n junction [18], therefore, the increase in MPV can be mostly attributed to an increase in depletion region of the sensor.

3.2 After irradiation

All the measurements presented below were performed in environmental chamber at -20°C in a dry atmosphere. This was done in order to control annealing of the irradiated device and reduce leakage current. All the post-irradiation measurements were performed on the same test chip as above. X-ray and MIP measurements contain results before standard annealing procedure (80 min at 60°C) [19], whereas linearity of response measurements were performed after annealing.

3.2.1 Linearity of response

Linearity was measured using the charge injection circuit for one of the HVStripV1 pixels with a linear transistor. In this case, a much more detailed scan was done by reducing step size of the input pulse height. The pixel output signal plot can be seen in figure 12. The input pulse height range was set to 0.3–1.9 V, and by assuming that the injection capacitance remained 0.62 ± 0.03 fF the equivalent charge corresponds 1100–7100 e^{-} . The assumption of the capacitance value had to be made because no reliable X-ray data were available after annealing to confirm its value. The non-linear behaviour seen in the plot within 0.3–0.9 V (1100–3400 e^{-}) range is attributed to the increase in noise level after irradiation and after annealing. The pixel signal was indistinguishable from noise within the injection range quoted previously. The error bars in the plot represent rms values of recorded pulse heights and indicate a level of noise. A linear relation is again observed starting from injection pulse height value of 0.9 V (3400 e^{-}), and the linearity is best illustrated by straight-line fit.

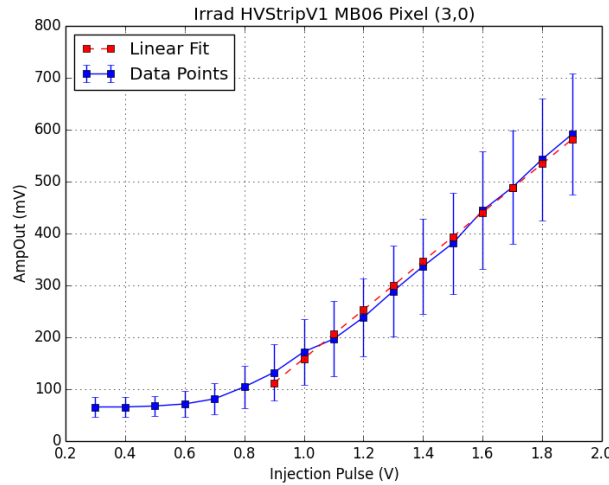


Figure 12. Pixel response to external charge injection after annealing. Due to increase in noise the linearity is only revealed after 0.9V ($\approx 3400 e^{-}$) injection pulse heights.

3.2.2 X-rays

The noise levels after irradiation were observed to significantly increase to 277 e^{-} and 386 e^{-} for pixels with linear and enclosed layout transistor respectively. The Fe-55 characteristic peak could no longer be observed. This meant that other X-ray sources with higher K_{α} photon energies were

needed. A variable X-ray source with Mo and Ag fluorescence targets, whose characteristic K_{α} photon energies correspond to 17.4 keV and 22 keV respectively, was used. The spectra were acquired for the two types of pixels at 60 V reverse bias and the results are shown in figure 13. For a pixel with a linear transistor Mo and for a pixel with an enclosed layout transistor Ag characteristic lines were used to determine the pixel gain. The gain values for each pixel were compared before and after irradiation. Table 1 gives a summary of results, where it can be seen that a drop in gain was observed for both pixels. The irradiation had a more severe effect on the pixels with enclosed layout transistors, therefore, a higher threshold had to be used during the measurements.

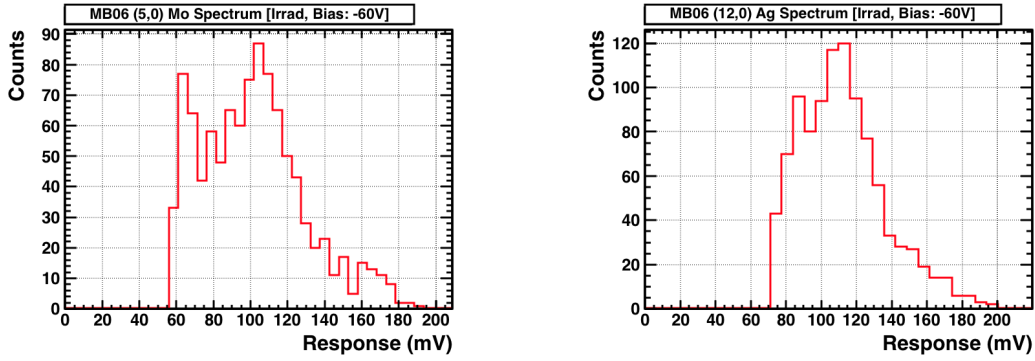


Figure 13. Spectra of Mo and Ag characteristic X-rays taken after irradiation for a pixel with a linear transistor (left) and for a pixel with an enclosed layout transistor (right) respectively.

Table 1. Pixel gain change due to irradiation. A more significant shift was observed for a pixel with an enclosed layout transistor in the preamplifier circuit. The gain values before irradiation had to be estimated at a higher feedback resistance VNFB value, which was used for post-irradiation measurements. The adjustment enabled us to match the DAC settings before and after irradiation.

| Pixel (c,r) | Before (mV/fC) | After (mV/fC) | Change (%) |
|-------------|----------------|---------------|------------|
| (5,0) | 147.4 | 132.7 | -10.0 |
| (12,0) | 150.6 | 112.1 | -25.6 |

3.2.3 MIPs

A set of MIP measurements was performed within 10–80 V reverse bias range for both pixel types. As for other measurements the increase in noise demanded a higher trigger level. As a consequence a part of a MIP spectrum was cut off and the MIP peak was not observed until 60 V and 70 V reverse bias was applied to a pixel with a linear transistor and for a pixel with an enclosed layout transistor respectively. In order to make a direct comparison of the change in peak position after irradiation the MPVs were extracted from the dataset taken at 70 V bias for both pixels. The comparison plots are shown in figure 14. As before, X-ray measurement data was used for calibration. One can observe from the histograms that there is a significant increase in signal for both pixels, which suggests that the depletion region is larger after irradiation for the same bias voltage. The notable increase in width of the MIP signal distribution could partially be attributed to a significant increase in noise

observed after irradiation. Another contribution to the increase in width could possibly come from trajectories of β^- particles emitted from the Sr-90 source not being perfectly perpendicular to the detector's surface. Given the nature of charge deposition by a MIP, varying angles of MIP paths in the sensor would result in a larger spread of the amount of charge deposited in the sensitive region. The significance of this effect on the shape of a MIP signal distribution requires further studies.

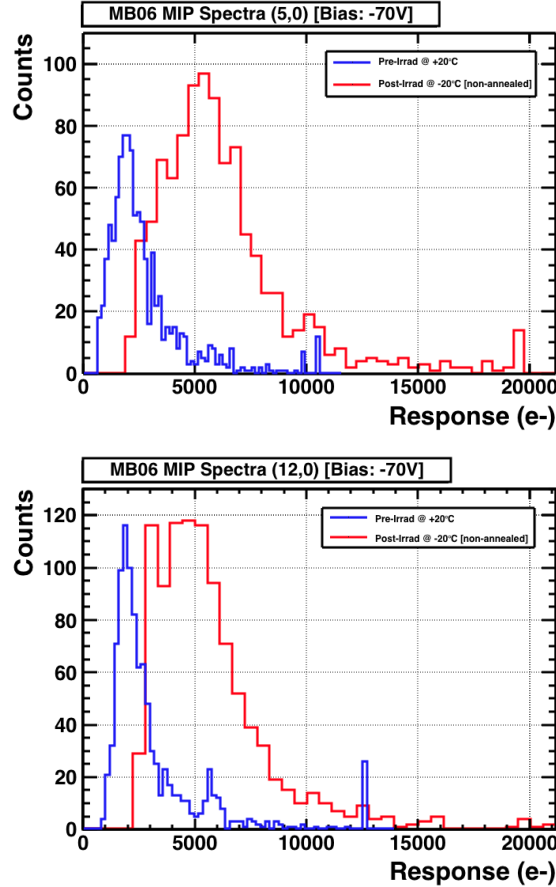


Figure 14. Comparison of MIP spectra before and after irradiation. A significant increase in MIP signal can be seen for both pixel types. The upper plot represents a pixel with a linear transistor, while the lower — a pixel with an enclosed layout transistor. The notable increase in width of the MIP peak is in part could be attributed to the increase in noise.

The summary of MIP peak position change before and after irradiation is given in table 2, where it is shown that the MPV is ≈ 2.8 times higher for a pixel with a linear transistor and ≈ 2.4 times higher for a pixel with an enclosed layout transistor. The SNR before annealing was also determined for both pixels and corresponds to 16.3 and 10.8 for these pixels respectively. Another study was done by a different research group on a HV-CMOS prototype chip manufactured in the same process as HVStripV1 [20]. The study investigated the change in average MIP induced charge collection and the change in the active region width as a function of the fluence received during irradiation. The results showed about a threefold increase in the active region width at 60 V bias after irradiation to $1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. About a twofold increase in the average charge collected

was observed for the same irradiation fluence and bias voltage. The study also contain simulation results which showed that the similar increase in the MIP signal is expected for a HV-CMOS sensor with substrate resistivity of $20 \Omega \cdot \text{cm}$ after irradiation to $\approx 1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ due to acceptor removal process.

Table 2. MIP peak position change after irradiation. Both datasets were taken at 70 V reverse bias.

| Pixel (c,r) | Before (e^-) | After (e^-) | Ratio |
|-------------|------------------|-----------------|-------|
| (5,0) | 1622 | 4513 | 2.78 |
| (12,0) | 1735 | 4178 | 2.41 |

4 Conclusions

The key point of the results presented here is that active pixels of HV-CMOS test chip “HVStripV1” were able to detect a clear MIP spectrum after irradiation to a fluence level of $1.2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. However, an increase in noise from $75 e^-$ to $277 e^-$ and from $85 e^-$ to $386 e^-$ was observed for pixels with linear and enclosed layout transistors respectively. The likely cause of this is the damage done to the bulk and preamplifiers during irradiation. The results suggest an increase in depletion region for a given bias after irradiation, which resulted in SNR values of 16.3 and 10.8 before annealing for the corresponding pixels. A similar increase in the depletion region after irradiation to $1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ was also observed by another research group for a HV-CMOS prototype chip manufactured in the same process as HVStripV1. The study by the research group showed that an increase in depletion region could potentially be attributed to an acceptor removal process in low resistivity p-substrate during irradiation. The most severely affected pixel of HVStripV1 after irradiation was the one with an enclosed layout transistor. This is an unexpected result and needs further investigation since a pixel group with enclosed layout transistors is expected to be more radiation-hard. Another important result is that the preamplifier’s linear behaviour is still preserved over a wide input charge range after receiving fluence levels expected in the HL-LHC environment.

Acknowledgments

The financing for postgraduate research student position comes from joint University of Glasgow and University of Oxford David McNaught scholarship. The support and financing for the research in part comes from UK Science and Technology Facilities Council (STFC). The research also received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025. Irradiation campaign at the University of Birmingham was supported by the H2020 project AIDA-2020, GA 654168. Gratitude also goes to J. A. Wilson, K. Parker, P. Dervan, the staff of University of Birmingham irradiation facility, for efficient operation and support.

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